HIGH EFFICIENCY 11 WATT OCTAVE S/C-BAND PHEMT MMIC POWER AMPLIFIER

J.J. Komiak, S.C. Wang, T.J. Rogers
Sanders, A Lockheed Martin Company
Nashua, NH 03061

Abstract

Design and performance of 0.25 um double fully selective recess PHEMT power amplifiers that have established new benchmarks for octave band power and efficiency is reported. The amplifers tested from two lots, ten wafers total, average 11 Watts at 42 % PAE with 17 dB power gain from 3 to 6 Ghz, with peak performance of 17 Watts at 54.5 % PAE and yields of 49.9 %.

Introduction

Power amplifiers have historically been a most difficult development problem. Resolution of conflicts inherent in simultaneously achieving high power with high efficiency with an inherently nonlinear device requires innovation. When wide bandwidth and cost are considered, the situation is complicated further. In this paper we descibe the design and performance of a high efficiency wideband power amplifier that is producible and low cost by employing a reproducible fully selective recess etch fabrication technology. The amplifier employs an off-chip output matching network on a high dielectric constant material, resulting in cost reduction and performance improvement compared to a fully-monolithic approach.

PHEMT Device

The PHEMT MMICs were fabricated using a 0.25 um double-recess double etch-stop fully selective process, evolved from our previously reported device structure [1]. This process is key to achieving the results presented here. The double-recess provides the higher breakdown voltage critical to achieving high power with excellent efficiency, while the self-limiting nature of the etch-stop results in uniformity and high yield. The PHEMT structure, shown in Figure 1, consists of a AlGaAs/GaAs superlattice buffer, a Si uniform doped AlGaAs layer below the channel and Si planar doping above the InGaAs channel. Spacer layers are utilized to reduce impurity scattering. Between both the Si-doped GaAs contact/Si-doped GaAs recess and the Si-doped GaAs recess/Si-doped AlGaAs gate interfaces, a thin etch stop layer has been added. The selective etch used in gate recessing stops at these precise depths. This technique has been implemented in all our PHEMT processes and has significantly improved yield and electrical uniformity. Figure 2 summarizes the extremely uniform DC parameters of the 0.25 x 200 um PCM test device measured on the 10 wafers from the two lots. The maximum variation in peak transconductance is less than 8 %.

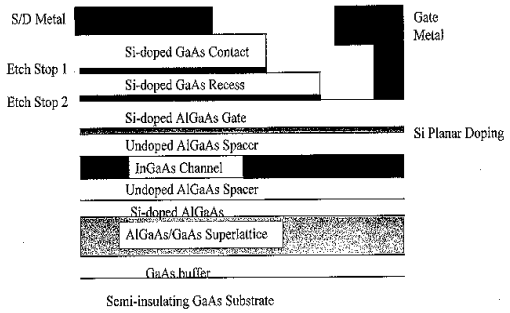

Figure 1: Fully Selective Double Recess 0.25 um Power PHEMT Structure

Circuit Design

Power amplifiers have always been a difficult and costly component to develop, due to inadequacy of models and measurement tools. To overcome this, a comprehensive methodology was employed in this design using small-signal models, optimum load and optimum source data, thermal analysis via ANSYS, and EM simulation via Sonnet. A small cell of 2 mm periphery (10 fingers x 200 um) was employed which alleviated the problems with large-periphery devices. Characterizing large periphery devices is inadequate for several reasons: the inability to

0-7803-4603-6/97/$5.00 (c) IEEE

accurately measure the low impedances of large periphery power devices, the thermal effects when operating CW in the small-signal regime during the characterization process,stability problems when presenting narrowband matching impedances to high gain broadband devices. Data taken on the 2 mm cell includes I/V curves, small signal S-parameters, optimum source and optimum load impedances, and power sweeps under the optimum loading conditions. A limited amount of harmonic load pull measurements were also performed. In this case, the second harmonic was terminated with impedances near the edge of the Smith chart, while the third and higher order harmonics were resistively terminated. Figure 3 summarizes the power performance of the 2 mm cell at the class AB bias point of Vds=7 Volts, Vgs=-0.5 Volts, with an optimum efficiency load. From the data, it is evident that the harmonically terminated case significantly enhances power-added efficiency [2].

The matching networks for the amplifier, the input, interstage, and output, were designed considering small-signal and power transfer simultaneously. The two-stage MMIC consists of four 2 mm cells

Wafer #	Idss	Gm	BVgd	Vp	Imax
	(mA)	(mS/mm)	(V)	(V)	(mA)
95-38-1E-1	40.1	338	>-25	-0.80	82.0
95-38-1E-2	41.4	334	-24.5	-0.78	81.7
95-38-1E-3	36.9	341	-23.5	-0.74	78.2
95-38-1E-4	41.6	323	-23.0	-0.84	81.6
95-38-1E-5	40.0	346	-23.0	-0.76	83.0
95-38-1E-6	44.6	310	-23.0	-0.93	80.7
95-38-1E-7	43.2	313	-24.5	-0.89	79.8
95-04-1E-2	44.7	346	-21.5	-0.85	87.2
95-04-1E-4	41.2	365	-19.8	-0.76	87.1
95-04-1E-6	37.1	345	-22.8	-0.68	82.4

Figure 2: DC Parameters of 0.25 x 200 um PCM Test Device

F(GHz)	Term.	P_{out} (W/mm)	Gain(dB)	PAE(%)
3	No	0.51	15.4	67
6	No	0.50	13.1	65
3	Yes	0.54	15.9	84
6	Yes	0.56	13.7	82

Figure 3: Power Performance of 0.25 um x 2 mm Device Cell

driving sixteen 2 mm cells for a total 0.25 um gate periphery of 40 mm. The input network was simulated for both small-signal response and power transfer of 50 ohms to the optimum source impedance. The interstage was simulated with both small-signal and optimum load of the 8 mm driving stage to optimum source of the 32 mm output stage power transfer. The output network used power transfer from the optimum load of the 32 mm output stage to 50 ohms and recognizing the problems with wide bandwidth, harmonic termination was employed only at S-Band and C-Band. The output matching consists of an off-chip output matching network (OCMN) on lapped and polished high dielectric constant Magnesium Calcium Titanate material (MCT-50). This results in cost reduction and performance improvement compared to a fully-monolithic approach [3]. Avoiding the constraints of 4 mil GaAs allows optimization of material Q, reducing output matching network losses and leading to improvement of power output and power-added efficiency. DC losses to the output stage are further reduced by employing 300 uinches of Au plate. The use of the OCMN reduces the area of the MMIC portion of the amplifier, increasing per wafer yield and lowering cost. The entire OCMN was simulated as a seven port network using Sonnet EM. The junction temperature of the amplifier was analyzed in ANSYS using finite element analysis, resulting in a 111 degrees C peak junction temperature with a 40 degrees C module baseplate temperature. Several unique features were employed in the circuit design of this amplifier: the use of RLC feedback to enhance stability, the use of loss to mitigate the change in input impedance from small to large signal of the power PHEMT caused by the high gate voltage swing which forward biases the gate-source diode. Standard techniques such as gate and odd-mode stabilization resistors were also employed.

Measured Performance

Figure 4 shows the HPA assembled on a Au-plated Silvar test carrier. Chip size is 4.65 mm x 6.15 mm x 0.1 mm and yield of amplifiers tested from two lots, ten wafers total, ranged from 36.7 % to 65.6 %, and averaged 49.9 %, summarized in Figure 5. Figure 6 and Figure 7 show the measured Power Output and PAE vs frequency of a typical test sample with a constant power

input of 23 dBm. Power output averaged across frequency is 11 Watts with an average power-added efficiency of 42 % and over 17 dB of power gain. The best samples achieved spot frequency performance of 17 Watts with PAE of 54.5 %, as shown in Figure 8 and Figure 9. This data was obtained using an automated pulse power test system under conditions of a pulse width of 500 usec and a duty cycle of 25 %. Figure 10 and Figure 11 show the measured CW Power Output and PAE vs Power Input at 4.8 GHz of a typical test sample with a constant power input of 23 dBm. Power output is 12 Watts with a power-added efficiency of 44.5 % and 16.8 dB of power gain. Compared to the amplifier reported in [4], these amplifiers achieve higher power and broader bandwidth, with equivalent efficiency even over the narrowband frequency range of 4.3 to 5.1 Ghz.

Acknowledgment

This work was sponsored by Lockheed Martin Government Electronic Systems, Moorestown, New Jersey.

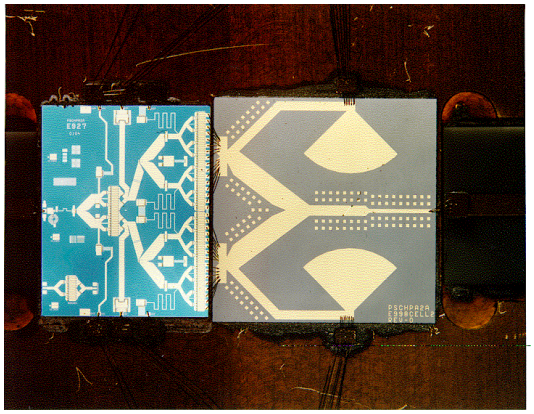

Figure 4: Photograph of High Efficiency Octave S/C-Band PHEMT HPA

Wafer #	Amplifiers	Yield (%)
95-38-1E-1	84	65.6
95-38-1E-2	45	35.2
95-38-1E-3	66	51.6
95-38-1E-4	47	36.7
95-38-1E-5	73	57.0
95-38-1E-6	54	42.2
95-38-1E-7	82	64.1
95-04-1E-2	63	49.2
95-04-1E-4	57	44.5
95-04-1E-6	68	53.1
Total	639	49.9

Figure 5: Yields of S/C-Band PHEMT HPA

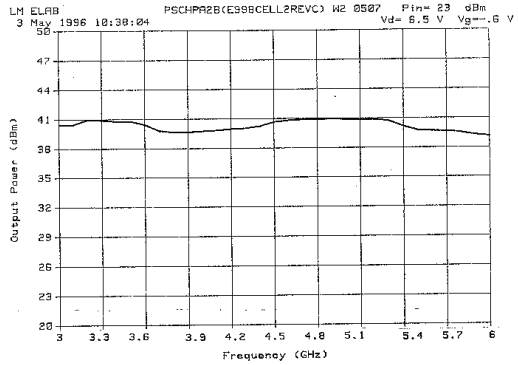

Figure 6: Typical Measured Power Output vs Frequency of S/C-Band PHEMT HPA

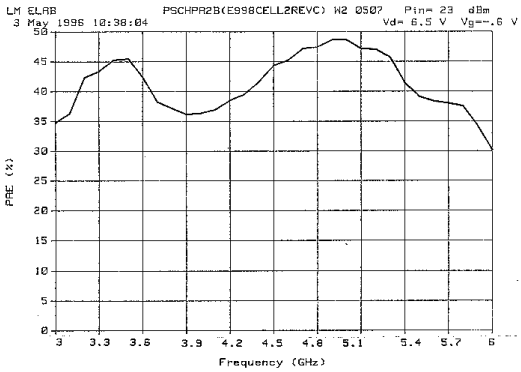

Figure 7: Typical Measured Power-Added Efficiency vs Frequency of S/C-Band PHEMT HPA

References

[1] S. T. Fu, W. F. Kopp, M. Y. Kao, K. H. G. Duh, P. M. Smith, P. C. Chao, T. H. Yu, "4 Ghz High Power High Efficiency Pseudomorphic Power HEMT," 1993 IEEE MTT-S Digest, 1469-1472.

[2] D. M. Snider, "A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier," IEEE Transactions, Vol ED-14, No 12, December 1967, pp 851-857.

[3] J. J. Komiak, D. Helms, "High Efficiency 20 Watt S/C-Band Power Amplifier MMIC," 1992 IEEE GaAs IC Symposium Digest, pp 187-190.

[4] P. M. White, T. M. O'Leary, "A 50% Efficiency 8 W C-Band PHEMT Power MMIC Amplifier," 1995 IEEE GaAs IC Symposium Digest, pp 277-280.

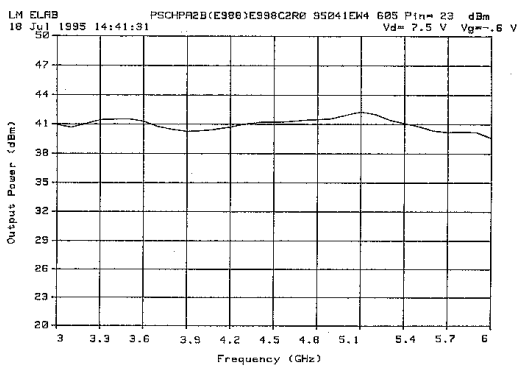

Figure 8: Best Measured Power Output vs Frequency of S/C-Band PHEMT HPA

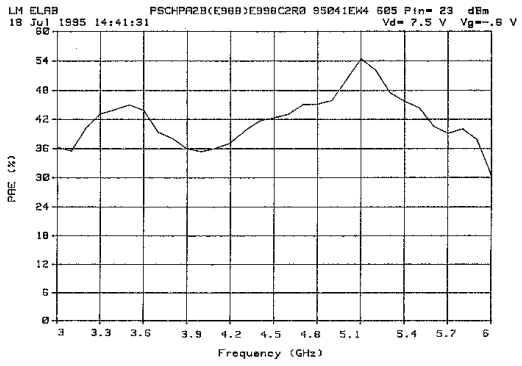

Figure 9: Best Measured Power-Added Efficiency vs Frequency of S/C-Band PHEMT HPA

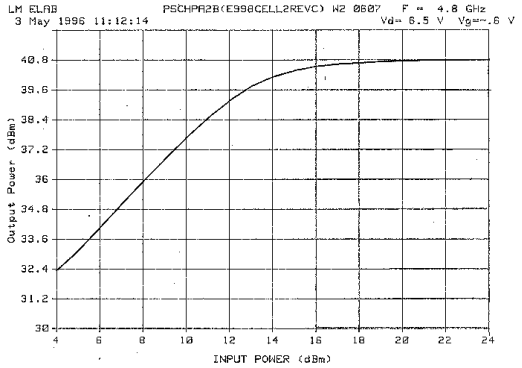

Figure 10: Typical Measured Power Output vs Power Input of S/C-Band PHEMT HPA

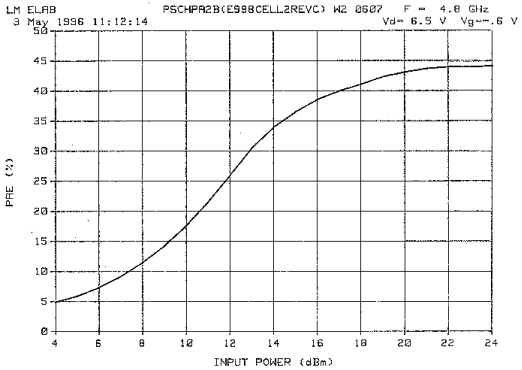

Figure 11: Typical Measured Power-Added Efficiency vs Power Input of S/C-Band PHEMT HPA